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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/574,445	04/06/2007	William A. Steer	GB 030183	9666
24737	7590	03/17/2010	EXAMINER	
PHILIPS INTELLECTUAL PROPERTY & STANDARDS			CHOW, YUK	
P.O. BOX 3001			ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/574,445	STEER ET AL.	
	Examiner	Art Unit	
	YUK CHOW	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on ____.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-17 is/are pending in the application.
 - 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) Claim(s) ____ is/are allowed.
- 6) Claim(s) 1-9, 13 and 17 is/are rejected.
- 7) Claim(s) 10-12 and 14-16 is/are objected to.
- 8) Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on ____ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. ____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. ____ .
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application
Paper No(s)/Mail Date ____ .	6) <input type="checkbox"/> Other: ____ .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-9, 13 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Sekiya et al.(US 6,583,775).

As to **claim 1**, Sekiya discloses an active matrix electroluminescent display device comprising an array of display pixels arranged in rows and columns, each pixel comprising:

an electroluminescent display element (Fig. 1(OLED));

a drive transistor (Fig. 1(TFT2)) for driving a current through the display element;

means (Fig. 1(TFT3)) for interrupting the drive of current through the display element; and

row driver circuitry (Fig. 2(22)) for generating control voltages to be applied to the pixels in each row in sequence including a drive voltage for the interrupting means,

wherein the row driver circuitry comprises a shift register arrangement (Fig. 2(24)) and logic arrangement (Fig. 2(23)) for generating the drive voltage for the interrupting means, the drive voltage for the interrupting means including a pulse having a duration which can be varied up to substantially the full field period less the address

period (Fig. 3, Stopping Control line duration can be up to full field period less than address period),

wherein the signal or signals propagated through the shift register arrangement control the pulse duration (Fig. 2(23, 24) control the pulse duration).

As to **claim 2**, Sekiya discloses the device as claimed in claim 1,
wherein the shift register arrangement and logic arrangement comprises first and second shift register devices, each having a pulse propagating through them, and logic means for deriving a signal having a pulse with duration derived from the difference in timing of the pulses propagating through the first and second shift register devices (Fig. 2(22, 23) both includes shift register, see Col. 11 line 40-Col. 12 line 6).

As to **claim 3**, Sekiya discloses the device as claimed in claim 2, wherein the pulse propagating in each shift register device has a duration corresponding the line time of the display (Fig. 3(scanning line X1)).

As to **claim 4**, Sekiya discloses the device as claimed in claim 2, wherein the logic means comprises a transmission gate which transmits a low pulse in response to a pulse on one of the shift register devices and transmits a high pulse in response to a pulse on the other one of the shift register devices (Fig. 2(VSP1, VSP2)).

As to **claim 5**, Sekiya discloses the device as claimed in claim 4, wherein the logic means further comprises a memory cell (Fig. 2(24) delay circuit inherently has memory cell) for maintaining a constant output between pulses received from the transmission gate.

As to **claim 6**, Sekiya discloses the device as claimed in claim 1, wherein the shift register arrangement and logic arrangement comprises first and second shift register devices, each having a pulse propagating through them, and logic means for deriving a signal having a pulse with duration derived from the duration of the pulse in one of the first and second shift register devices (Fig. 2(22, 23) both includes shift register, see Col. 11 line 40-Col. 12 line 6).

As to **claim 7**, Sekiya discloses the device as claimed in claim 6, wherein the pulse propagating in one shift register device has a duration corresponding to the line time of the display and the pulse propagating in the other shift register device has a duration for controlling the display element illumination period (Col. 12 lines 7-39).

As to **claim 8**, Sekiya discloses the device as claimed in claim 1, wherein the shift register arrangement and logic arrangement comprises a shift register device, having a pulse propagating through it having a duration dependent on the desired illumination time of the display element, and logic means for deriving from the shift register device a pulse having a duration corresponding to the line time of the display (Col. 15 line 56- Col. 16 line 24).

As to **claim 9**, Sekiya discloses the device as claimed in claim 8, wherein the logic means for deriving from the shift register device a pulse having a duration corresponding to the line time of the display comprises a combination element for combining the pulse at the output of one shift register element for one row with the pulse at the output of another shift register element for an adjacent row (see Fig. 8(28, 29)).

As to **claim 13**, Sekiya discloses the device as claimed in claim 1, wherein each pixel comprises drive transistor threshold compensation circuitry (see Fig. 1(CS, TFT3).

As to **claim 17**, Sekiya discloses a method of driving an active matrix electroluminescent display device comprising an array of display pixels arranged in rows and columns, in which each pixel comprises an electroluminescent display element, a drive transistor for driving a current through the display element and means for interrupting the drive of current through the display element, the method comprising:

propagating a pulse or pulses through a shift register arrangement (Fig. 3(VSP1));

using a pulse from the shift register arrangement to allow pixel addressing control voltages to be applied to the pixels of a row during an addressing period (Fig. 3(VSP2);

using the shift register pulse or pulses to derive a drive voltage for the interrupting means including a pulse having a duration which can be varied up to substantially the full field period less the addressing period (Fig. 3, Stopping Control line duration can be up to full field period less than address period); and

applying the drive voltage for the interrupting means to the interrupting means after the pixel addressing period (see Col. 12 lines 7-39) .

Allowable Subject Matter

3. Claims 10-12 and 14-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. The following is a statement of reasons for the indication of allowable subject matter:

Regarding **claim 10**, cited references does not teach or suggest: “a first pulse from the shift register arrangement and logic arrangement is combined with a first template control signal or signals (A1, A2) to provide a first control signal or signals (A1r,A2r) for the addressing of the pixel, and a second pulse from the shift register arrangement and logic arrangement is combined with a second template control signal (A3) to provide the drive voltage (A3r) for the interrupting means both during the addressing of the pixel and during subsequent driving of the pixel.”.

Regarding **claim 14**, cited reference does not teach or suggest: “the drive transistor threshold compensation circuitry comprises first and second capacitors (20, 22) connected in series between the gate and source of the drive transistor (24), a data input to the pixel being provided to the junction between the first and second capacitors (20, 22) thereby to charge the first capacitor (20) to a voltage derived from the pixel data voltage, and a voltage derived from the drive transistor threshold voltage being stored on the second capacitor (22).”.

Claims 11-12 and 15-16 are allowable, since they depend on claim 10 and 14 respectively.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YUK CHOW whose telephone number is (571)270-1544. The examiner can normally be reached on 8-6 M-TH E.T..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on 571 272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Y. C./
Examiner, Art Unit 2629

/AMARE MENGISTU/

Supervisory Patent Examiner, Art Unit 2629